AMENDMENTS

Please amend the above-identified application as follows:

In the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

1   1.   (Currently Amended) An apparatus for performing the addition of

2 propagate, kill, and generate recoded numbers, said apparatus comprising:

3   a circuitry configured to receive at least a first operand, a second operand, and

4 a carry-in bit, the first and second operands comprising respective first and second

5 propagate, kill, and generate recoded number representations of respective first and

6 second binary operands;

7   a first carry-save adder configured to add said first operand and said second

8 operand to generate a third propagate, kill, and generate recoded number

9 representation and a carry-out bit; and

10   a modified carry-save adder configured to receive the third propagate, kill, and

11 generate recoded number representation from the first carry-save adder, ~~the carry-out~~

12 ~~bit,~~ and the carry-in bit from the circuitry, add the separate propagate, kill, and

13 generate bits of the third propagate, kill, and generate recoded number representation

14 with the ~~carry-out bit and the~~ carry-in bit to generate a sum value and a carry value,

15 <u>wherein the circuitry provides the carry-out bit from the first carry-save adder at a first</u>

16 <u>output and the carry value from the modified carry-save adder at a second output</u>.

1   2.   (Original) The apparatus of claim 1, wherein said sum value and said

2 carry value are dual rail encoded values.

1   3-6.   (Canceled)

1   7.   (Currently Amended) A method for processing propagate, kill, and
2   generate representations of respective first and second binary operands, comprising:

1   receiving a carry-in value and a first and a second propagate, kill, and generate
2   representation of respective first and second binary operands;

3   <u>generating a third propagate, kill, and generate representation and a carry-out</u>
4   <u>value responsive to</u> ~~adding~~ the first and second propagate, kill, and generate
5   representations ~~to generate a third propagate, kill, and generate representation and a~~
6   ~~carry-out value;~~ and

7   ~~mathematically~~ <u>logically</u> combining the third propagate, kill, and generate
8   representation with ~~the carry-out value and~~ the carry-in value to generate a sum value
9   and a carry value<u>; and</u>

10   <u>providing the carry-out value, the carry value, and the sum value as a result of</u>
11   <u>the addition of the first and second propagate, kill, and generate representations.</u>

1   8.   (Currently Amended) The method of claim 7, wherein said step of
2   ~~mathematically~~ <u>logically</u> combining comprises adding the third propagate, kill, and
3   generate representation and the carry-in value.

1   9.   (Canceled)

1   10.   (Currently Amended) The method of claim 7, wherein said step of
2   ~~mathematically~~ <u>logically</u> combining further comprises generating dual rail encoded
3   values.

1   11-22. (Canceled)

1   23.   (New) The apparatus of claim 1, wherein the sum value is a function
2   of the third propagate representation and the carry-in value.

1   24.   (New) The apparatus of claim 23, wherein the sum value is the XOR
2   combination of the third propagate representation and the carry-in value.

1   25.   (New) The apparatus of claim 1, wherein the carry value is a function

2   of the third propagate representation, the carry-in value, and the third generate

3   representation.

1   26.   (New) The apparatus of claim 25, wherein the carry value is the OR

2   combination of the third generate representation with the AND combination of the

3   third propagate representation and the carry-in value.

1   27.   (New) The apparatus of claim 1, wherein the carry-out value is a

2   function of the first and second generate representations.

1   28.   (New) The apparatus of claim 27, wherein the carry-out value is the

2   OR combination of the first and second generate representations.

1   29.   (New) The apparatus of claim 1, wherein the circuitry provides the

2   sum value at a third output.

1   30.   (New) The method of claim 7, wherein said step of logically

2   combining comprises a XOR combination of the third propagate representation and

3   the carry-in value.

1   31.   (New) The method of claim 7, wherein said step of logically

2   combining comprises an OR combination of the third generate representation with the

3   AND combination of the third propagate representation and the carry-in value.

1   32.   (New) The method of claim 7, wherein said step of generating

2   comprises an OR combination of the first and second generate representations.